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Raytheon's Net-Centric Communications

Building a Foundation for Innovative Solutions



Raytheon

Customer Success Is Our Mission



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Design things and then see how they work. It is this passion that led Hendry to get his Bachelor of Science in electrical engineering from the Massachusetts Institute of Technology in 1975, and to continue with a career in engineering.

Now a 31-year veteran of Raytheon, Hendry is focusing on systems engineering for military satellite communication systems. Some of his major projects include working on HC3, the next generation of Army Satellite Communications terminals; HDR-RF, a U.S. Air Force program that has developed a very high-data-rate programmable modem for satellite communications; and Objective Gateway, another Air Force program to develop a family of gateways that will interconnect different types of communication systems.

A New Jersey native, Hendry is most proud of the work he did on the on the first generation of extra high frequency (EHF) satellite communications terminals for the U.S. Navy.

“We started with a clean sheet of paper and designed a terminal that implemented the most complex waveform devised up to that time,” Hendry explained.

The test with the first satellite was very successful, and this served as the foundation for Raytheon’s EHF SATCOM business.

Waveform Portability

Software-defined radios (SDR) are playing an increasingly important role in both military and commercial communications. There are two key characteristics of an SDR: 1) Some or all of the baseband or RF signal processing is accomplished through the use of software, and 2) The signal processing can be modified post-manufacture. One of the primary advantages of an SDR is the capability to operate with more than one waveform. Instead of the legacy paradigm in which each waveform required its own radio, an SDR can implement multiple waveforms by reconfiguring with the appropriate software.

In SDR usage, the term *waveform* is used to describe the entire set of radio functions that occur from the user input to the RF output, and vice versa. A waveform typically includes physical- and link-layer functions. Physical-layer functions on the transmit side typically include error correction coding, interleaving and modulation. The receive side includes the complementary functions, as well as time, frequency and spatial (antenna) tracking. Link-layer functions may include time or frequency division multiplexing as well as signaling protocols associated with allocating link-layer resources.

Although relatively simple, low throughput waveforms may be implemented almost entirely on general-purpose processors (GPP). The complex, high-throughput waveforms used for above-2 GHz satellite communications are generally implemented on a combination of GPPs, digital signal processors, and field-programmable gate arrays (FPGA).

The advent of SDR technology has led to the concept of waveform portability. There are two main goals for waveform portability:

1. A waveform developed for one platform (set of users) should be adaptable to a different platform with minimum changes.

2. It should be possible to port a waveform developed for one hardware implementation to a different hardware implementation with minimum changes.

The first goal implies platform independence — that a common waveform should not depend on the particulars of where and how it is used. For example, the U.S. Army, Navy and Air Force all use interoperable satcom waveforms, including the MIL-188-165A waveform and the LDR, MDR and XDR EHF waveforms. Since interoperability implies that the physical- and link-layer processing is compatible, it should not be necessary to develop different waveforms for each service. The key to achieving this waveform portability goal is defining the waveform boundary to exclude those components that depend on a particular platform. For example, while most waveform physical- and link-layer functions are identical among all platforms, the implementation of time, frequency and spatial tracking loops depends on whether a platform is stationary or mobile. This implies that the tracking loops themselves should be excluded from the waveform boundary and that the waveform should provide a generalized interface to the tracking loops. A commonality and variability analysis of waveform components across the full range of platforms is essential for defining the waveform boundary to maximize portability among different platforms.

The second goal implies hardware independence; a waveform implementation should depend as little as possible on the specifics of the hardware on which it executes. Advances in technology generally make a particular hardware configuration obsolete in only a few years, while waveforms have lifetimes measured in decades. When a new hardware configuration is developed to address the needs of a new application or to solve a technology obsolescence issue, it should be possible to

Portability will be an essential feature of future waveform designs

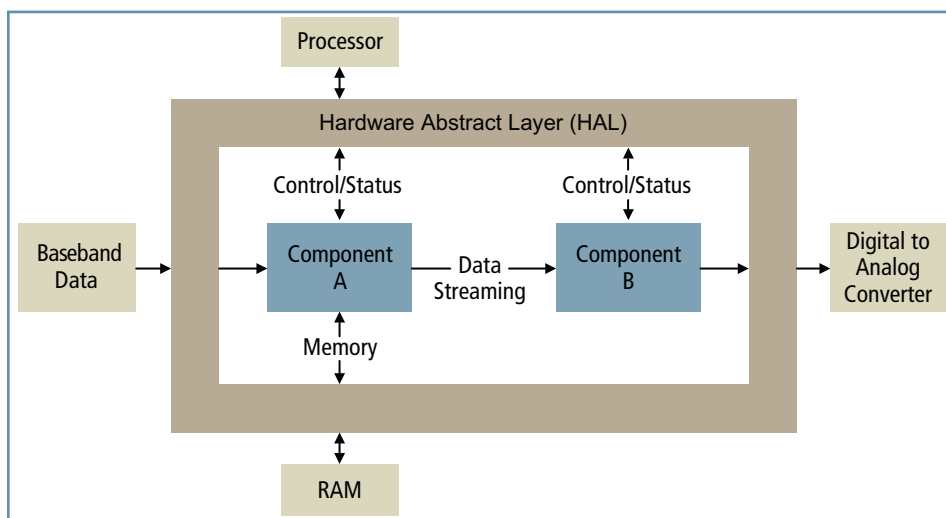


Figure 1. Hardware Abstraction Layer

use an already-developed waveform with a minimum number of changes. Since different applications may have different hardware configurations because of specific requirements, (e.g., cooling, form factor, environments) hardware independence is also important in achieving platform independence.

One of the keys to achieving hardware independence is the hardware abstraction layer (HAL). The concept of a HAL is best described by an example (Figure 1). Without a HAL, the designer of an FPGA waveform component that interfaces to external memory must account for the particular interface presented by that memory. This inherently makes the FPGA component dependent on the particular hardware implementation. Porting that waveform component to a different hardware module that uses a different type of memory requires changing the component accordingly. Hardware dependencies are not limited to external memory. Other interfaces, including data converters, processors, and interconnection paths present the same issues. A HAL presents a uniform interface to the FPGA component regardless of the hardware implementation. One side of the HAL implements the interface required by the specific hardware implementation. The other side of the HAL presents a uniform,

standardized interface to the waveform component. The developer of the hardware module is also responsible for developing the associated HAL that provides a standardized interface between waveform components and the specific features of the hardware module.

Analog-to-digital and digital-to-analog converters present a more complex problem for a HAL. Typically the waveform components that interface to these components, including modulators and demodulators, are designed with specific assumptions about sampling rate, resolution, and other performance characteristics of the data converters. In this case, the waveform must set minimum standards for the data converters in much the same way that it sets minimum standards for memory, FPGA resources and other processing resources. Even in this area, a HAL can significantly decouple the waveform from the hardware implementation. In this case the HAL takes the form of a sample rate conversion (SRC) function. This digital signal processing function converts between the actual sampling rate of the data converters (the hardware implementation) and the sampling rate expected by the waveform. Although the hardware implementation must meet minimum standards for data conversion to be suitable for

a particular waveform, the use of a SRC function in the HAL significantly enhances waveform portability.

In 2007, Raytheon demonstrated the critical concepts of waveform portability by porting the advanced extremely high frequency (AEHF) waveform to a hardware implementation different from that for which it had originally been designed. The AEHF waveform is among the most complex of waveforms in use today, with a number of features designed to provide anti-jam, low probability of intercept and high data-rate performance. In the past, such waveforms have typically been tightly coupled to a particular hardware implementation with memory, interconnection, data converter, and processor interfaces specific to that hardware. As part of this effort, a HAL layer was inserted between the waveform and the hardware implementation to decouple the waveform from the specifics of the hardware. The HAL includes an SRC function that mediates between the data conversion sample rates implemented by the hardware platform and the sample rates assumed by the waveform designers. This six-month effort resulted in an AEHF waveform implementation that is now portable by virtue of the standardized interfaces and HAL. This is essentially a one-time effort, now that the waveform itself is portable; few if any changes will be needed to port it to yet another hardware implementation that uses the same HAL construct.

This effort demonstrated that the additional work required to make a waveform portable is small compared to the benefits it provides. The effort would have been even less had it been done at the time the waveform was originally developed rather than afterward. Given the major advantages for both the developers and the users of waveforms, it is likely that design-for-portability will become more of a requirement for waveform development. ●

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